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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/806,136	03/26/2001	Kenichi Nakanishi	450106-02621	5076

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EXAMINER
ENCARNACION, YAMIR

ART UNIT	PAPER NUMBER
2186	9

DATE MAILED: 05/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/806,136	NAKANISHI ET AL.	
	Examiner	Art Unit	
	Yamir Encarnacion	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *10 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 7, 9-11, 13-15, 17-19, and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by *Estakhri* (USPN: 6,081,878).

Claimed	***Estakhri***
7. A nonvolatile memory system comprising:	See figure 1.
a plurality of nonvolatile storages	See figure 1, memory chips 18 and 20.
within which at least one cluster of data are [perhaps applicant meant "is"] recorded,	See figure 1, sub-block 44.
with each cluster constructed by a plurality of sectors;	See figure 1, the rows within sub-block 44.

address designating means for designating an address of the cluster in which data is recorded;	See figure 1, host 14. Column 1, lines 43-46 states that host "14 writes and reads information, organized in sectors, to and from memory bank 16 which includes a first nonvolatile memory chip 18 and a second nonvolatile memory chip 20."
recording means for recording data into a storage location at the address designated by said address designated means;	See figure 1, controller 12.
wherein,	
said plurality of storages are divided into a plurality of segments;	See figure 1, the block locations 42.
each said segment is distributed and arranged into said plurality of storages; and each said segment includes a group of continuous sectors of said plurality of storages.	The block locations 42 meet the limitation of the claim.

As to claim 9, data is immediately written in registers 22 and 32 of chips of chips 18 and 20 after data is transferred to chips 18 and 20.

As to claim 10, block (which reads on the claimed "segment"), chip address (whether chip 18 or 20 is desired), and row addresses would be necessary for writing to the correct location in the system described in figure 1 of *Estakhri*.

As to claims 11, 15, and 19, see the comments for claim 7 above.

As to claims 13, 17, and 21, see the comments for claim 9 above.

As to claims 14, 18, and 22, see the comments for claim 10 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Estakhri* (USPN: 6,081,878) in view of *Evers* (USPN: 6,542,975), DOS, and the FAT file system.

Claimed	***Estakhri***
7. A nonvolatile memory system comprising:	See figure 5.
a plurality of nonvolatile storages	See figure 5, non volatile memory units 508.

within which at least one cluster of data are recorded, with each cluster constructed by a plurality of sectors;	In *Estakhri*, each block (which reads on the claimed "cluster") includes 32 sectors in the preferred embodiment. See column 7, lines 45-48.
address designating means for designating an address of the cluster in which data is recorded;	Column 7, lines 55-57 states that "[a]n actual LBA received from host 504 (a host-provided LBA) identifies a sector of information."
recording means for recording data into a storage location at the address designated by said address designated means;	See figure 5, controller 510.
wherein, said plurality of storages are divided into a plurality of segments; each said segment is distributed and arranged into said plurality of storages; and each said segment includes	Not shown.

a group of continuous sectors of said plurality of storages.	Figure 13 shows that each block 1302 includes a group of continuous sectors of the storages 670 and 672. Column 18, lines 22-25 state that "each of the first and second row-portions 1310 [this is a typo, 1310 should be construed to mean 1313], 1312 includes storage for 512 bytes of data information." Later column 18, lines 28-30 states that each "of the first row-portions 1310 [this should read 1313] includes an even sector field 1314 for storing an even sector (S0, S2, S4, . . .)" Column 18, lines 31-33 states that each "of the second row-portions 1312 includes an odd sector field 1318 for storing odd sector (S1, S3, S5, . . .) of information." It should be obvious that sectors S0, S1, S2, S3, S4 mentioned above are continuous.

Estakhri does not clearly show the details which relate to the claimed "segments." Stated otherwise, *Estakhri* does not explicitly disclose that the non volatile memory described therein is

partitioned. However, *Estakhri* explains that solid state devices such as the one described therein are used in place of conventional hard disks. See column 1, lines 35-37. *Evers* explains on column 1, lines 42-54 that conventional hard disks are partitioned into one or more partitions. *Estakhri* and *Evers* do not explain why hard disks are partitioned.

The examiner takes "Official notice" that the operating system DOS and its file system FAT were known prior to the filing of the present application. A person of ordinary skill in the art would have found it obvious to format the solid state devices described by *Estakhri* using FAT for the purpose of making the solid state devices described by *Estakhri* compatible with the very popular operating system known as DOS.

A common reason for partitioning a disk formatted using FAT prior to the filing of the present application was to improve disk usage given that cluster size was dependent on the size of the partition. Accordingly, a person of ordinary skill in the art would have found it obvious to partition the solid state device described by *Estakhri* into multiple partitions for the purpose of improving disk usage.

A different reason those of ordinary skill in the art chose to partition their storage into multiple partitions was because they desired to keep data separate from applications so as to make backups easier (since data tends to change often but applications do not). Still another reason those of ordinary skill in the art chose to partition their storage into multiple partitions was for the purpose of using multiple operating systems each requiring its own partition because they each had their own unique file system (Like a system having Window NT which used the NTFS file

system, the Linux operating system which used one of the many unix file systems (UFS, ext2, minix, etc.), the Windows operating system which used the FAT file system). Any one of the reasons explained above would have motivated those of ordinary skill in the art to partition the solid state device described by *Estakhri* into multiple partitions.

A solid state disk like the one described by *Estakhri* partitioned into multiple partitions would have met the limitation requiring that "said plurality of storages [be] divided into a plurality of segments" where the partitions read on the claimed "segments."

Also, because "a partition is [typically] organized as a linear sequence of clusters" (See *Evers*, column 1, lines 42-54) and because the blocks in *Estakhri* (which read on the claimed "clusters") are "distributed and arranged into said plurality of storages." A partition in *Estakhri* organized as a linear sequence of blocks as suggested by *Evers* would be "distributed and arranged into said plurality of storages" because of the "distributed" nature and the arrangement of the blocks in *Estakhri*.

Finally, because the partitions in the environment described by *Estakhri* would have included blocks and because --as was explained above-- the blocks in *Estakhri* include a group of continuous sectors, it necessarily follows that the partitions would have included a group of continuous sectors.

As to claim 9, data is immediately written in registers 671 and 673 of chips of chips 670 and 670 after data is transferred to chips 670 and 672.

As to claim 10, partition (which reads on the claimed "segment"), chip address (whether chip 670 or 672 is desired), and sector addresses would have been necessary for writing to the correct location in the system described in figure 13 of as modified in the *Estakhri/Evers/DOS/FAT* combination.

As to claims 8, 12, 16, and 20, the portions of the LBA-PBA map 800 shown in figure 8a of *Estakhri* that would have corresponded to each partition read on the claimed conversion table.

As to claims 11, 15, and 19, see the comments for claim 7 above.

As to claims 13, 17, and 21, see the comments for claim 9 above.

As to claims 14, 18, and 22, see the comments for claim 10 above.

5. In the alternative, claims 8, 12, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Estakhri/Evers/DOS/FAT* as applied to claims 7, 11, 15, and 19 above, and further in view of the admitted Prior Art.

Assuming arguendo that *Estakhri/Evers/DOS/FAT* does not explicitly describe that "an access is performed with reference to a logical cluster address/physical cluster address conversion table that is formed for **each** segment," (Emphasis added) then

Page 10, lines 3-11 of the specification as originally filed explains that "according to the [prior art] flash memory, since a logical/physical address conversion table is constructed [for] every segment, it is necessary to refer to the logical/physical address conversion table upon accessing. Therefore, like an [sic] example mentioned above, when four clusters are

simultaneously written over four segments, a memory for holding address conversion tables of four segments is needed."

A person of ordinary skill in the art would have found it obvious to have an address conversion table for each partition ("segment") given that the admitted prior art teaches that each partitions needed one.

As to claim 12, 16, and 20, see the comments for claim 8 above.

Response to Arguments

6. Applicant's arguments filed March 10, 2003 have been fully considered but they are not persuasive.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Yamir Encarnacion by phone at (703) 308-5466.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any formal response to this action intended for entry should be mailed to Box AF, Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 746-7238 and labeled "EXPEDITED PROCEDURE." Any informal or draft communication should be faxed to (703) 746-7240 and labeled "INFORMAL" or "UNOFFICIAL" or "DRAFT" or "PROPOSED" and followed by a phone call to the Examiner at the above number. Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

YEE

Yamir Encarnacion

Patent Examiner

May 15, 2003

MATTHEW KIM
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